Laboratory 3

D/A AND A/D CONVERTERS

Purpose: The study of ADC and DAC with application on an integrated 8 bit ADC and an R-2R DAC.

Summary of theory

a) The conversion relationship; characteristic features.

The analog-to-digital converters (ADCs) convert a voltage (analog value) into a number proportional to that voltage, while the digital-to-analog converters convert a number into an analog voltage proportional to that number. The two devices have complementary functions, thus the transfer function of the DAC, $f_{DAC}: Z \rightarrow R$, is the inverse of the transfer function of the ADC, $f_{ADC}: R \rightarrow Z$.

The correspondence between the number and the voltage, valid for both devices, depends on the reference voltage, V_{REF} as in relation (1), formula which is named *the conversion relationship* of the ADC or the DAC:

$$V_0(N) = N \cdot V_{REF} = \left(\sum_{k=1}^{n} b_k 2^{-k} \right) \cdot V_{REF} \qquad (1)$$

One can observe that for all N, $V(N) < V_{REF}$. Therefore, N is a positive number ($N < 1$). We write the binary number in its natural form in natural binary code:

$$N_{NB} = b_1 b_2 .. b_n$$

where b_1 is the most significant bit (MSB), and b_n is the least significant bit (LSB). n represents the number of bits of the DAC. The fractional number $N < 1$ is represented as follows:

$$N_{NB} = 0,b_1 b_2 .. b_n$$

and it can be calculated based on the natural number $N > 1$:

$$N = N_{NB} / 2^n$$

The difference between the voltages corresponding to 2 successive numbers is called *resolution*, and it corresponds to a "quantum" of voltage:

$$V_{LSB} = V_{REF} / 2^n$$

The voltage corresponding to the maximum number which can be represented using n bits is called *full scale voltage.* It is one quantum lower than V_{REF}.

$$V_{FS} = V_{REF} - V_{LSB} = V_{LSB} \cdot (2^n - 1)$$

Based on those notations, you can write the conversion relationship as in the table:

Table 1 - The truncation characteristic

$[0, V_{LSB})$	000…00
$[V_{LSB}, 2\ V_{LSB})$	000…01
$[2V_{LSB}, 3V_{LSB})$	000...10
…	…
$[V_{REF} - 2\ V_{LSB}, V_{REF} - V_{LSB})$	111…10
$[V_{REF} - V_{LSB}, \infty)$	111…11

Table 2 - The roundoff characteristic

$V(N)$	N_{NB} (n bits)
$[0, \frac{1}{2} V_{LSB})$	000…00
$[\frac{1}{2} V_{LSB}, \frac{3}{2} V_{LSB})$	000…01
$[\frac{3}{2} V_{LSB}, \frac{5}{2} V_{LSB})$	000...10
…	…
$[V_{REF} - \frac{5}{2} V_{LSB}, V_{REF} - \frac{3}{2} V_{LSB})$	111…10
$[V_{REF} - \frac{3}{2} V_{LSB}, \infty)$	111…11

Table 1 corresponds to a conversion relationship with *truncation*. Usually, one uses a conversion relationship with *roundoff*, as in Table 2, where all the values are shifted lower with $V_{LSB}/2$. For example, the combination 000…01 is obtained between $V_{LSB}/2$ and 3 $V_{LSB}/2$, etc. You will find the multiples of V_{LSB} *in the center* of the steps, *not at their edges.* The ADC0804 converter that is used has a roundoff characteristic.

Obs: The maximum value ∞ from the table cannot, in fact, be greater than the maximum value specified in the converter's *datasheet*, otherwise it can be damaged.

b) The static transfer function and the global errors

The ideal characteristic of an ADC is shown in Fig. 1, plotted with dotted line (you can obtain the characteristic of the DAC by switching the axes of coordinates).

The errors of a real conversion characteristic from an ideal characteristic are:

- the offset (zero) error: the conversion characteristic does not intersect the origin of the axes (Fig.1a);

- the gain error (the scale factor error): the conversion characteristic does not intersect the full scale, after the offset error correction (Fig.1b);

- the non-linearity error (Fig.1c), errors that are still present after the correction of the previous two errors:

  - the integral non-linearity error: the maximum difference between the theoretical input voltage, corresponding to a number from the output of the ADC (from the mathematical model), and the voltage you obtain from the measurement in that case;

  - the differential non-linearity error: the maximum difference between the theoretical resolution of the ADC (from the mathematical model), and the resolutions you measure for each number ($|\delta V_{theoretical} - \delta V_{measured}|$).

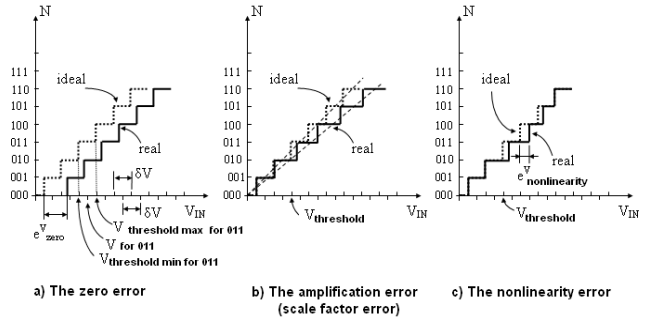

Fig.1. The errors of the ADCs.

c) The operation of the R-2R ladder DAC

The R-2R resistor ladder DAC is the most used DAC.

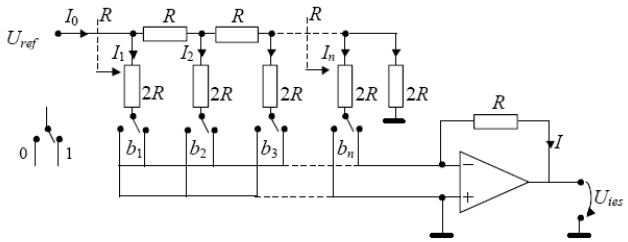

Fig.2. R-2R ladder DAC.

One can observe that, at any point of the resistive network, the equivalent resistance you see to the right side, is R (see the dotted line arrows on Fig.2). Therefore, each current will, successively, become half of the precedent current:

$$I_1 = I_0/2, I_2 = I_1/2 = I_0/4, .. I_i = I_0/2^i$$

The bits are represented as switches that allow the flow of the currents I_i to the summing node (the inverting input, (-), of the Op. Amp.), when they are on logical "1". The same conversion relationship (1) is obtained.

d) The operation of the successive approximation ADC (SA)

The SA ADC is the most commonly used medium speed ADC. The schematic of this ADC is shown in Fig. 3.

- the logical signal "start of conversion", SC = 1, commands the start of a conversion cycle. The end of the conversion cycle is reported by the signal "finish conversion", FC=1. Connect

SC and FC together to obtain continuous conversion, the conversion cycles succeeding one after another.

- a conversion cycle for *n* bits and a clock $T_{CK}=1/f_{CK}$ takes:

$$T_{CONVERSION}=n \cdot T_{CK} \qquad (2)$$

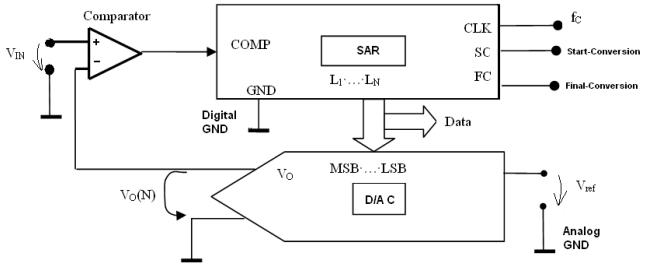

Fig.3. ADC with SA

During each clock period, the comparator compares the input analog voltage V_{IN} (the voltage that one wants to convert to a binary number) to the voltage provided by the DAC at that moment. Because of the DAC existent in the structure of the ADC, this is called a "feedback" converter. The voltage provided by the DAC, $V_0(N)$ has its value given by the relation (1).

SAR operates sequentially with a fixed clock frequency f_{CK}, generating the numbers *N,* following the successive approximation algorithm. The algorithm is presented below, for the particular case of n=8 bits.

The successive approximation algorithm

- **STEP 1:**

After the command "start conversion" (the signal *SC=1*, that can usually be asynchronous with f_o), synchronous with the first rising slope of the clock pulse, SAR generates, at its output, the test binary number:

$$N_1 = 10000000$$

Corresponding to that number, at the output of the DAC the voltage is:

$$V_0(N_1) = V_{REF} \cdot \sum_{i=1}^{8} b_i \cdot 2^{-i} = \frac{V_{REF}}{2}$$

The logical signal *COMP,* from the output of the comparator, is the result of the comparison of the voltages V_{IN} and $V_o(N_1)$*:*

$$\text{COMP} = c_1 = \begin{cases} 0, & \text{if } V_0(N_1) > V_{IN} \\ 1, & \text{if } V_0(N_1) \le V_{IN} \end{cases}$$

At the next rising slope of the clock signal, the SAR stores the logical value of that comparison (c_1), overwriting the bit b_1, for the rest of the conversion cycle (the test value "1" is replaced by the final value c_1).

You can see the decision of the bit b_1 *as the determination of the interval to which the input voltage* V_{IN} *belongs,* $\left[0,\frac{V_{REF}}{2}\right)$ *or* $\left[\frac{V_{REF}}{2},V_{REF}\right)$.

- **STEP 2:**

Simultaneous with that new slope of the clock signal, the SAR sets the second bit, next to the MSB, to the test value $b_2=1$, so that the number from the output of the SAR is:

$$N_2=c_1 1000000$$

c_1 being the result from the preceding step; this produces at the output of the DAC the corresponding voltage:

$$V_0(N_2)=V_{REF}\cdot\sum_{i=1}^{8}b_i\cdot 2^{-i}=V_{REF}\cdot(c_1\cdot 2^{-1}+1\cdot 2^{-2})$$

The result of the comparison of the voltages V_{IN} and $V_0(N_2)$, at the second step of the algorithm is:

$$\text{COMP}=c_2=\begin{cases}0, & \text{if } V_0(N_2)>V_{IN}\\ 1, & \text{if } V_0(N_2)\le V_{IN}\end{cases}$$

The result is stored and b_2 is overwritten.

- **STEP 3**

The SAR tests the next bit $b_3=1$, the next number from the output of the SAR being

$$N_3=c_1\, c_2 100000$$

(the index of number N is simultaneously the approximation step and the index of the bit to be determined), the procedure being the same as in steps 1 and 2.

The algorithm continues until all the bits, from MSB to LSB, are determined. The larger the number of bits, the better the approximation $V_o(N)\approx V_{IN}$.

The quantization error resulting from applying this algorithm is:

$$e_q=\delta V=\pm\frac{1}{2}V_{LSB}=\pm 2^{-(n+1)}\cdot V_{REF}.$$

The algorithm is completed when the value for the least significant bit, LSB, is determined. At this moment, the result is stored in the SAR and the signal FC is set.

e) The quantization error; the quantization noise; the signal-to-noise ratio

Generally the quantization error of an ADC is the difference between U_x and the voltage given by the resulting number $V(N_X)$:

$$e_c= U_X-V(N_X)$$

This error can be seen as a random variable – a quantization *noise* with variance:

$$\sigma_c^2= q^2/12$$

where q is the quantum: $q = V_{LSB}$. The root-mean-square (RMS) voltage corresponding to this noise is:

$$U_{\text{noise RMS}} = q/\sqrt{12} \qquad (3)$$

The signal-to-noise ratio SNR (or *SINAD: Signal to Noise and Distorsion*), which includes the effect of all noise sources, including analogue noise, quantization noise and the harmonic distortions, is defined as:

$$\text{SNR}_{\text{tot}}\,[\text{dB}] = \text{SINAD}\,[\text{dB}] = 20\lg\,(U_{\text{RMS signal}} / U_{\text{RMS noise + harmonics}})$$

The connection between the SNR_q (quantization) and the number of bits is:

$$n = \log_4 2/3 + \log_4 \text{SNR}_q^2$$

Transforming the SNR in dB and replacing in the formula, one obtains:

$$n = (\text{SNR}_q[\text{dB}] - 1.75) / 6.02 \qquad (4)$$

Measurements

Remark: You must bring a calculator with you!

A. Studying the ADC in steady state

Use the ADC from Fig. 3, based on the ADC0804 integrated circuit, as in the schematic from Fig. 4. The diodes D_8, D_9 and the resistor R are for input protection. R and C_2 also act as a Low Pass Filter which eliminates the high-frequency perturbations. The group R_8, C_1 establishes the oscillation frequency of the internal oscillator. The supply voltage of 5V is obtained from the output of a 3-terminal voltage regulator (LM7805 or LF50).

Pay attention! Before supplying the circuit, verify, using the voltmeter from the multimeter, the polarity of the 2 wires of the supply.

Set the supply to 9V (6V are not enough for 7805 to output 5V). Verify that the (+) of the supply is connected at the red connecting screw of the breadboard, and the red plug is connected to the pin 1 of the 3-terminal voltage regulator. Verify that at the output of the voltage regulator (V_{CC}), connected to the horizontal group of holes, the voltage is V_{DC}=5V. Observe the correspondence between the schematic and the circuit on the breadboard.

Verify that:

- Do not confuse V_{supply} (9V) with V_{DC} (5V), you risk burning the chip!
- All bits (pins 11-18) are connected through the wires to the 8 corresponding LEDs. If 4 bits are connected to the 4 resistors of the R-2R DAC (which you do not use at this point), remove them from the resistors and connect them to the LEDs. Pay attention to the correct order of the wires! LSB corresponds to DB0 (pin 18), and to the right most LED!
- The 390Ω resistance from the input of the ADC (pin 6) is connected, through the blue wire, to pin 2 of the trimmer potentiometer P_1.
- For measuring V(N)m the potentiometer's cursor must be connected also to the green terminal of the breadboard (V_{IN}), where the DC digital voltmeter is also connected.
- the pins 3 (*Write*) and 5 (*Interrupt*) have functions equivalent to SC, FC respectively, and you must connect them together for continuous conversion. If the conversion does not start (nothing happens when adjusting P_1), you should connect them for a short time to GND, through a wire (equivalent to the switch SW_1 on the schematic, component which does not

exist on the test board). Remove the wire after several seconds – ***equivalent to applying a start impulse.*** Usually, it is enough to remove and then connect back the supply of the board in order to start.

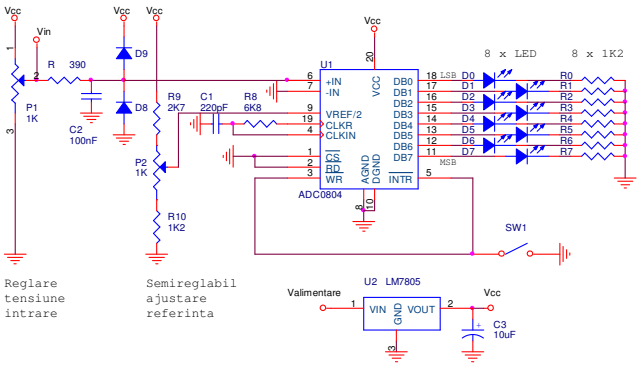

Fig.4. The schematic of the ADC built on the breadboard.

- The 2 grounds (analog – AGND for the input, and digital – DGND for clock, outputs DB0-DB7 and LEDs) are separated on the board: the analog GND is on the upper row, whereas the digital one is on the lower row. The two groups of holes are connected at the leftmost side of the test board, **in only one point**.

1. Viewing the operation of the ADC

View the clock oscillator of the ADC, by connecting the scope at pin 19. Read the frequency f_0 indicated by the scope (C_1 and R_8 can differ from the values in fig. 4). Calculate the internal frequency f_{CK}, which is 8 times smaller (this value is a particularity of the circuit ADC0804 and is taken as is; other circuits can divide the clock differently). Compute the conversion time T_{conv0} of the ADC using relation (2).

Measure the conversion time of the ADC, T_{conv_meas}, meaning the time duration between two negative impulses of the SC (pin 3 of ADC0804).

Compute the theoretical number of conversions per second $1/T_{conv\ meas} = f_{s\ \text{meas}}$. This is measured in Hz, but it is usually denoted in Sa/s (samples per second, which is the same thing). Compare to f_s in Sa/s written on the front panel of the scope; what type of ADC does the oscilloscope use?

Compute the maximum frequency of a sinusoidal signal $f_{sine\ max\ 1}$ whose samples can be converted with this ADC.

2. Calibration of the ADC

- Connect the DC voltmeter on pin 9, where the value $V_{REF}/2$ must be.
- Adjust P_2 finely until you obtain this value.

Based on V_{REF} and n=8b compute the values V_{LSB} and V_{FS}.

3. Determination of the ADC static conversion characteristic and its errors

Apply to the ADC the input voltages V_{IN}, so that you can measure the *main code transitions*, when all bits, of the binary code, change, starting from a certain bit. For example, 00011111→00100000 is a main transition.

In order to achieve the main transitions, measure, using the indication of the 8 LEDs on the breadboard and the digital voltmeter, the voltages $V_{IN}(N)$ which by conversion produce the respective transitions (in *ascending* order); for example for the number 0010 0000:

- Starting from a smaller voltage, slightly **increase** the input voltage until the LEDs show this binary combination. On the voltmeter, read the corresponding V_{IN}.
- Compute also the theoretical value $V_0(N)$:

$$V_0(N) = NV_{LSB} - V_{LSB}/2$$

Using these results determine the maximum nonlinearity error (integral).

Compute and measure also the voltage corresponding to the transition 254→255 (V_{FS}, all LEDs are on).

B. Study of the ADC+DAC in dynamical regime (variable V_{in}).

Create a conversion chain: the generator, the ADC, the DAC and the oscilloscope (fig. 5). Instead of the continuous voltage given by P1 (*steady-state* regime), use a sinusoidal signal from the generator, of frequency 30Hz (*dynamic regime*), that will be digitized by the DAC and converted again to an analog signal, by the ADC. For the ease of measurement, you will use a 4 bit DAC, connected to *the most significant* 4 bits of the existing ADC, so that the voltage resolution is greater (worse) than before.

Proceed as follows:

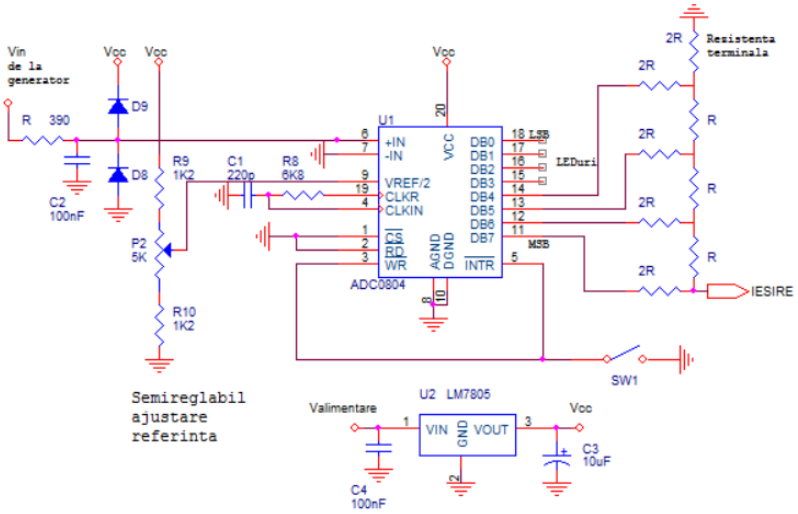

Fig. 5 Connecting the input of the ADC to the generator and the output (only 4 bits) to the input of the R-2R DAC

- ***Do not apply the alternative voltage from the generator and the continuous voltage***

from P1 simultaneously! Remove the wire that connects the cursor of P1 to the input terminal of the ADC (the terminal of the 390Ω resistance having the other terminal at pin 6). Remove the voltmeter from the breadboard (the green plug, connected through a wire to the 390Ω resistance); for now, the generator stays unconnected, until its level is properly set.

- Identify on the board the resistances R and 2R on the scheme, as well as the terminal resistor.
- Disconnect the most significant 4 bits (pins 11-14, 11 being MSB) from the LEDs and connect them to the inputs of an R-2R DAC, using the white wires, as in the scheme from figure 6.

Verify that the MSB is the one that is the furthest from the *terminal* resistance 2R from the GND (drawn in the upper right part on the scheme in fig. 6). ***Pay attention!*** Pins 15-18 stay connected to the LEDs.

Apply the variable input signal as follows:

- Connect the generator of sinusoidal signal of frequency f=30Hz directly to the scope with *Cy=1V/div*. For the ease of measurement, set the zero level of the scope in the center of the screen.
- We want to generate a signal with peak-to-peak values between [0 .. V_{FS}].

  Compute the ***new V_{FS} and V_{LSB}*** for V_{REF}=*4.096* and *n=4b!*
- On the generator, set the peak-to-peak output voltage to V_{FS}= V_{REF}-V_{LSB} [V_{PP}]

computed before, and set the offset to half of this value; this assures us that the signal takes only positive values – it DOES NOT decrease below the 0V level on the scope. You need to obtain a signal which ***is completely inside the dynamic range of the 4 bit ADC***, as in fig. 6, otherwise you will not obtain the expected result.

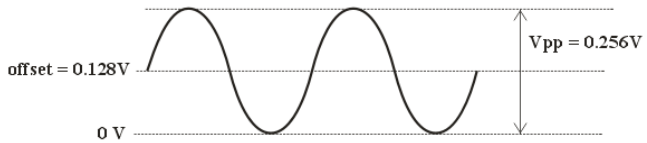

Fig. 6 Input signal for the ADC-DAC chain.

4. Viewing the waveform from the output of the DAC

Connect the sinusoidal signal generator, set as before, to the *input* of the ADC (the green plug connected to the 390Ω resistance – the input will look as in Fig. 5).

Connect the scope to the OUTPUT terminal from the DAC, in fig. 5 (the resistance 2R that is the furthest from the *terminal* resistance from GND). You should see, at the output of the DAC, a sine approximated by 2^4=16 voltage levels, of peal-to-peak value denoted $V_{FS\ DAC}$, which is measured using the cursors. *OBS:* if the input signal does not look exactly as in fig. 6, the output signal will not have 16 levels!

Obs: *if no waveform is observed, it is possible that the ADC is not "on"; in this case, you can either remove and connect back the supply, or apply a* ***starting impulse****, as in point A (temporary short-circuit between pins 3 or 5 and GND)*

Why does the maximum peak-to-peak value from the output of the DAC differ from the maximum peak-to-peak value from the input of the ADC? Indication: check the DAC scheme.

Slightly adjust **VERTICAL POSITION** to place the image symmetrically on the display. Choose C_x in order to have one period of the signal on the display. Press the **RUN/STOP** knob of the scope to count the steps (in **STOP** mode). If there are less than 16 steps or the signal is limited or distorted, press again the knob (to be in **RUN** mode) and ***very slightly*** adjust the amplitude and the offset, from the generator, until you obtain exactly 16 steps, and the image resembles the most a sine formed of steps. Do the 2 settings alternatively, probably more than once. Draw the obtained image.

Obs: If you adjust the amplitude/offset too coarsely, you will probably not be able to adjust the image by observing the waveform at the *output*, because it is too distortioned; in this case, re-attach the scope to the *input* and repeat the adjustments as before.

For the 4 bit DAC with V_{REF}=*5V*, calculate the theoretical values corresponding to the steps 0 (V_o), 1 (V_{LSB}), 2, 4, 8, and 15 (V_{FS}).

In the **STOP** mode, measure, using the cursors, the values of these steps. For precision measurements, you can modify C_y=*0.1V/div* (x10 zoom effect on vertical axis), and alternatively change the function of the **VERTICAL POSITION** knob (position on Y / the cursors, pressing, successively, **CH1 Menu** and **Cursor**) in order to place on the step you want to measure. Compare the values you measure with the ones you calculated (the theoretical ones). Name some sources of errors.

Explain why were the steps 0,1,2,4,8,15 required and not others.

5. Verify the tracking speed of the ADC-DAC chain

Set the **RUN** mode and C_y=*1V/div*, and verify that you have 16 steps on the display.

Increase the frequency of the signal to 1000Hz. Observe that a period of the signal is now approximated by only a few samples (steps). Which is the number of steps N_{steps}? In the **STOP** mode, using the time cursors, measure the width of a step T_{step}. Draw the image. Compare $T_{conv\ meas}$ and T_{step}. Explain the connection between them. *Obs: n=8b*, even though we only use 4, the converter does not "know" this!

Explain why when the frequency increases, the number of steps decreases.

6. The effect of the number of bits on the quantization noise

a) Go back to the frequency of 30Hz on the generator, in order to have 16 steps again. Connect the scope to the ***input in the ADC*** (the sinusoidal signal of amplitude as in fig. 6) and display a few periods on the screen, making sure that the image does not exceed the upper/lower edge of the screen. Set the sope in FFT mode (**Math Menu → Operation FFT**). Set C_x=50Hz/div, 10dB/div.

Obs: the scope cannot compute the FFT correctly if the image in time domain does not contain enough periods and is not correctly displayed on the screen. The scope is not a spectrip analyzer, the computation of the FFT is done on the image displayed in time!

The scope in FFT mode displays RMS values, in dB (0dB = $1V_{RMS}$).

Using the cursors (**Cursor->Source Math->Type Magnitude**), measure the value of the fundamental component in dB, $U_{RMS\ noise}$ (the cursor will be placed approximately in the superior part of the noise „band").

Using the frequency cursors, measure the frequency of the fundamental component (**Type -> Frequency**).

Compute the SNR $U_{RMS\ meas}$ / $U_{RMS\ noise}$ (in dB – what happens to a *ratio* when it is requested in dB?)

Measure using the distortionmeter (in parallel with the oscilloscope) the THD factor and from here obtain the SINAD in dB for this input signal; compare to the calculated one, based on the two values in dB.

b) Move the scope and the distortionmeter at the ***output of the DAC***, view in time domain the signal that has 16 steps (finely adjust the generator if there are not exactly 16 steps or the signal is not symmetric). Move back to FFT mode with C_x=50Hz/div, 10dB/div. Usinf the cursors measure the amplitude of the fundamental component in dB and the *maximum* RMS value of the spectral components of the noise, which now is a total noise (quantization+analog).

Compute the ratio $U_{RMS\ meas}$ / $U_{RMS\ noise}$ in dB. Measure SINAD in dB with the distortionmeter (- THD_{dB}) and compare them.

Compute, based on $V_{LSB\ DAC}$, the value of the RMS voltage of the quantization noise $U_{noiseRMScalc}$ – see relation (3). Convert the result in dB and compare to the noise measured (approximately) on the screen.

Compute SNRq [dB] from relation (4), for n=4b. Compare the value with the measured SINAD (obs: SNR_q does not take into account the analog noise).

Disconnect the oscilloscope from the output of the DAC, short-circuit the scopes' terminals and measure with the cursors (**Cursor->Source Math->Type Magnitude**) the RMS value of the analog noise, $U_{RMS\ analog\ noise}$, having as source the input stage in the scope and the disruptive voltages from the cable.

How do you interpret this value in the context of the above computations?

c) Move to a 3 bit DAC. For that, connect the LSB wire of the DAC on 4 bits to GND, instead of connecting it to pin 14 of ADC0804 (DB4) from fig. 5.

What do you notice when moving from 4 to 3 bits? Explain.

Verify the no. of steps on the scope for 3 bits (without drawing).

Do the measurements from the table again for 3 bits (pay attention to the new V_{LSB})!

Obs: At the end of the lab, bring the board to the initial state: connect again all the 8 LEDs to the ADC, redo the connection of the ADC's input to the P1 cursor, as in point 1 (fig. 4).

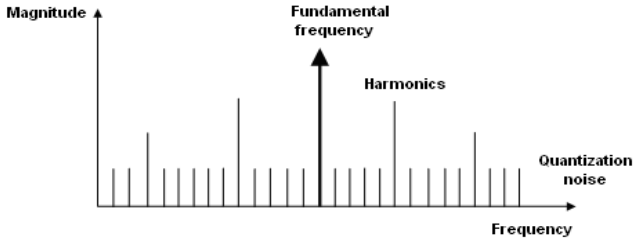

Fig.7. The spectrum of the output signal of the ADC-DAC chain

Preparatory questions:

1. a) Given an 8 bit SA ADC, with V_{REF} = 10.24V, calculate V_{LSB}, V_{MSB}, V_{FS} and the resolution.

b) Apply the SA algorithm and determine the output number, for U_{IN} = 7V, the truncation case.

c) Repeat b) for roundoff.

2. What is the voltage obtained at the output of an 8bit DAC, V_{REF}=10V, for the input number N=5DH? Without repeating the computation, which is the voltage for N'=5EH?

3. Explain the difference between a unipolar ADC and a bipolar one. What is the dynamic range of the input voltage for each of them (as function of V_{REF})? Is the studied ADC unipolar or bipolar?

4. Determine the value of the quantization error for a 12 bit DAC, with a reference voltage of V_{REF} = 10.24V.

5. Name the error sources for the R-2R DAC.

6. Define the main transitions. Why are they important when measuring a(n) ADC / DAC?

7. What should be the conversion time of an ADC-DAC chain in order to correctly display the waveform from point 4, from measurements (16 steps for a sine at 1000Hz)?

8. How much should the minimum frequency of an 8 bit SA ADC be in order to use it at the quantization of a voice signal for telephonic transmission (the signal is supposed to have f_{max}= 3.4kHz)?

9. Define the offset error for a unipolar DAC.

10. Search on the Internet the ADC0804 *datasheet* and study it.